Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

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1. (Presently Amended) A method of translating instructions, said method comprising:

translating a first block of instructions executable in a first processor architecture, into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; and

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of code; and

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.

2. (Canceled) ~~The method as claimed in claim 1, said method further comprising:~~

~~adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.~~

A1

3. (Presently Amended) The method as claimed in claim 1~~2~~, wherein said instruction added to said first block of instructions, branches to correction code if said expected TOS is not equal to said actual TOS.

4. (Original) The method as claimed in claim 3, said method further comprising:

determining if execution of instructions in said first block of instructions changes the actual TOS.

5. (Original) The method as claimed in claim 4, said method further comprising:

in response to determining execution of instructions in said first block of instructions changes the actual TOS, adding an instruction to an end of the first block of instructions to update the actual to TOS.

6. (Presently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, said set of instructions,

which when executed by a processor, cause said processor to perform a method comprising:

A1

translating a first block of instructions executable in a first processor architecture, into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; ~~and~~

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of code; and

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.

7. (Canceled) ~~The computer-readable medium as claimed in claim 6, wherein said set of instructions further includes additional instructions, which when executed by said processor, cause said processor to perform said method further comprising:~~

~~adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.~~

8. (Presently Amended) The computer-readable medium as claimed in claim 67, wherein said instruction added to said first block of instructions, branches to correction code if said expected TOS is not equal to said actual TOS.

9. (Original) The computer-readable medium as claimed in claim 8, wherein said set of instructions further includes additional instructions, which when executed by said processor, cause said processor to perform said method further comprising:

determining if execution of instructions in said first block of instructions changes the actual TOS.

10. (Original) The computer-readable medium as claimed in claim 9, wherein said set of instructions further includes additional instructions, which when executed by said processor, cause said processor to perform said method further comprising:

in response to determining execution of instructions in said first block of instructions changes the actual TOS, adding an instruction to an end of the first block of instructions to update the actual to TOS.

11. (Presently Amended) A system comprising:

a first unit of logic to translate a first block of instructions executable in a first processor architecture, into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; and

A1

a second unit of logic to generate an expected Top of Stack (TOS) position in said stack for said first block of code, wherein said second unit of logic further adds at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.

12. (Canceled) ~~The system as claimed in claim 11, wherein said second unit of logic further adds at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions.~~

13. (Presently Amended) The system as claimed in claim 112, wherein said instruction added to said first block of instructions, branches to correction code if said expected TOS is not equal to said actual TOS.

A1

14. (Original) The system as claimed in claim 13, wherein said second unit of logic determines if execution of instructions in said first block of instructions changes the actual TOS.

15. (Original) The system as claimed in claim 14, wherein said second unit of logic, in response to determining execution of instructions in said first block of instructions changes the actual TOS, adds an instruction to an end of the first block of instructions to update the actual to TOS.